Document Title

128K x 8 Hight Speed SRAM with 3.3V Central Power

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	September 12,2001	
0B	Add B (36-pin TF-BGA 6x8mm) and H (32-pin TSOP-1 8x13.4mm) package type	June 20,2002	

128K x 8 HIGH-SPEED CMOS STATIC RAM 3.3V REVOLUTIONARY PINOUT

FEATURES

- High-speed access times:
  8, 10, 12 and 15 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
  – 32-pin 300mil SOJ
  – 32-pin 400mil SOJ
  – 32-pin 400mil TSOP-2
  – 32-pin TSOP-1 (8mmx13.4mm)
  – 36-pin TF-BGA (6mmx8mm)

DESCRIPTION

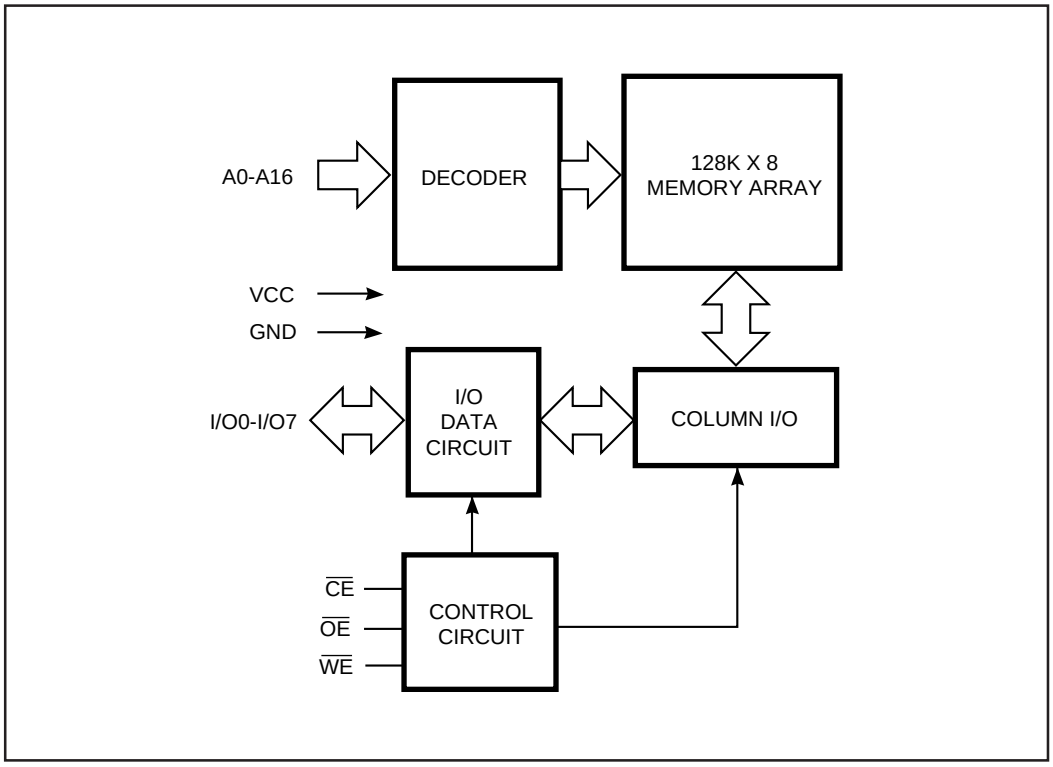
The *ICSI* IC63LV1024 is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The IC63LV1024 is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

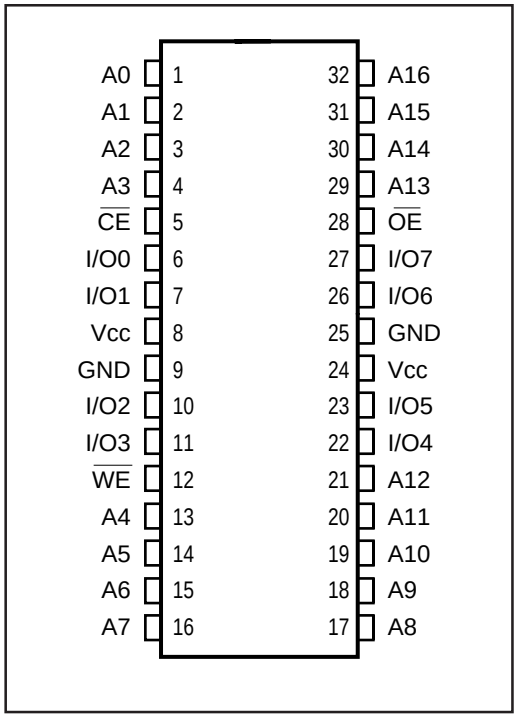
The IC63LV1024 operates from a single 3.3V power supply and all inputs are TTL-compatible.

The IC63LV1024 is available in 32-pin 300mil SOJ, 400mil SOJ, 400mil TSOP-2, TSOP-1 (8mmx13.4mm), and 36-pin TF-BGA (6mmx8mm).

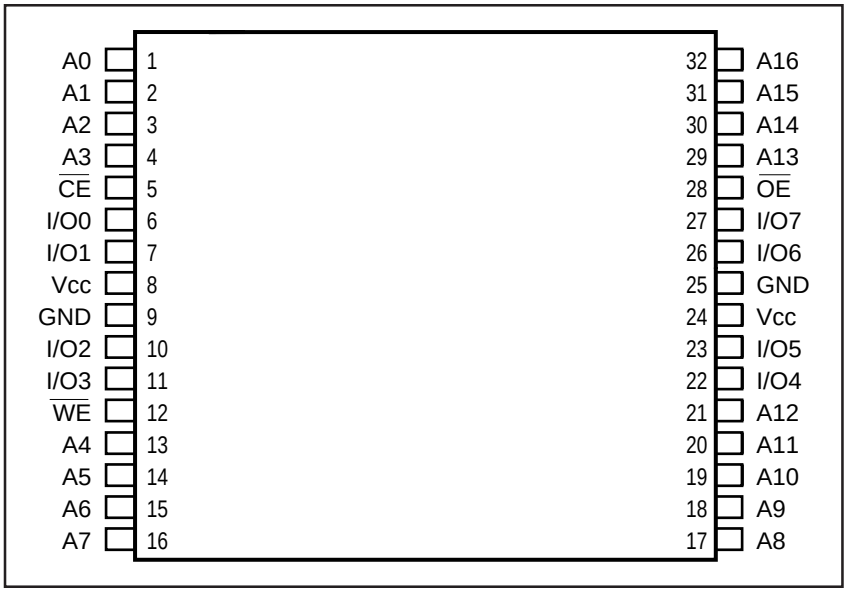
FUNCTIONAL BLOCK DIAGRAM



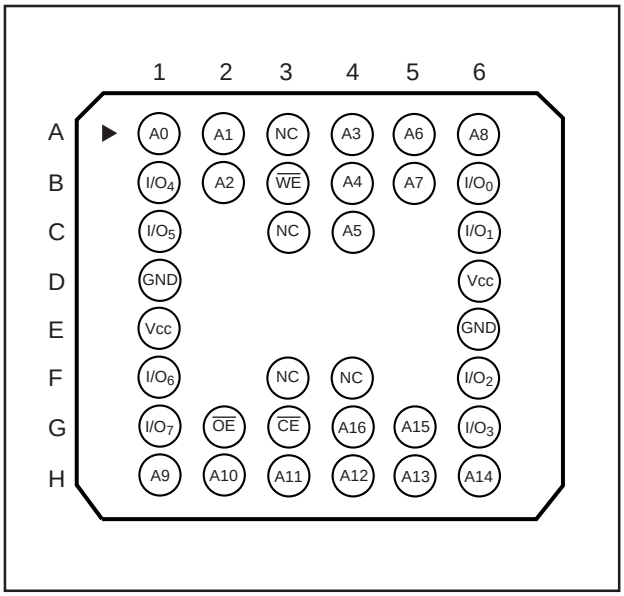
PIN CONFIGURATION
32-Pin SOJ



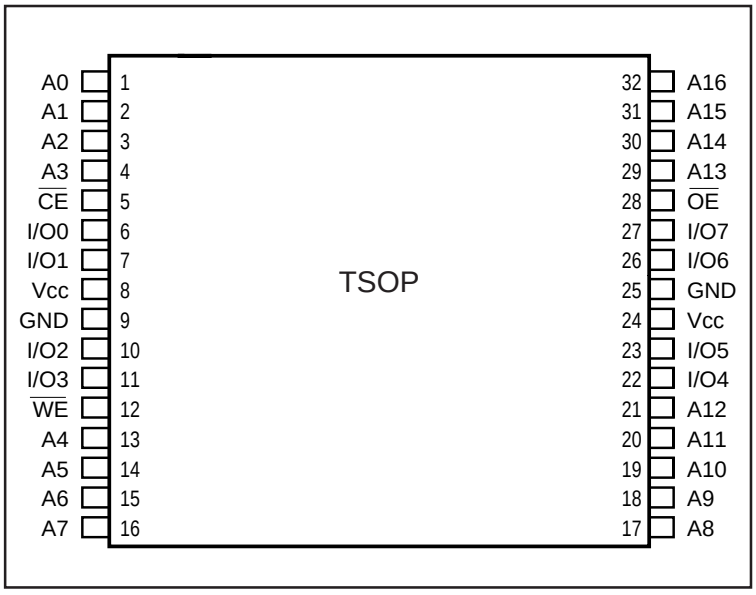
PIN CONFIGURATION
32-Pin TSOP-2



PIN CONFIGURATION
36-Pin TF-BGA (TOP View)
(6mm x 8mm)



PIN CONFIGURATION
32-Pin TSOP-1
(8mm x 13.4mm)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O1-I/O8	Bidirectional Ports
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	3.3V ± 0.3V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–2 –5	2 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com. Ind.	–2 –5	2 5	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.
2. The Vcc operating range for 8 ns is 3.3V +10%, -5%.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-8 ns		-10 ns		-12 ns		-15 ns		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = Max.	Com. Ind.	— —	160 170	— —	150 160	— —	140 150	— —	130 140	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	30 40	— —	30 40	— —	30 40	— —	30 40	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≤ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— —	10 15	— —	10 15	— —	10 15	— —	10 15	mA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-8 ns		-10 ns		-12 ns		-15 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	—	6	—	7	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	4	0	5	0	6	0	7	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	4	0	5	0	6	0	7	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b

Notes:
1. The Vcc operating range for 8 ns is 3.3V +10%, -5%.

AC TEST LOADS

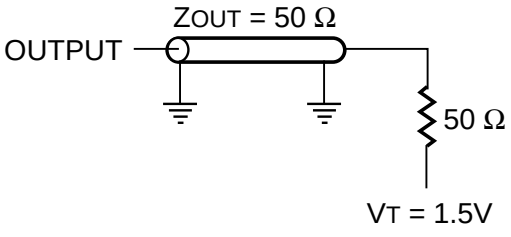


Figure 1a.

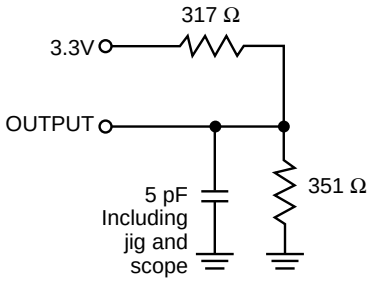
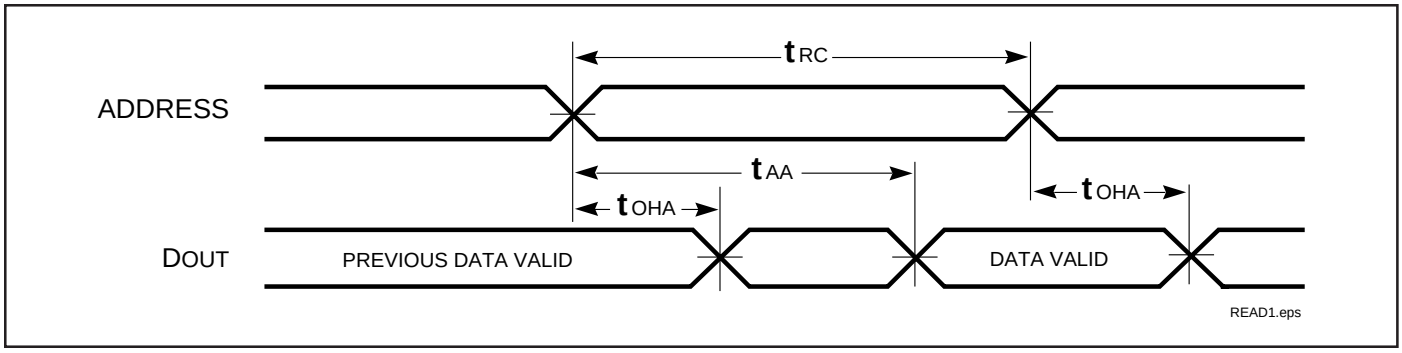


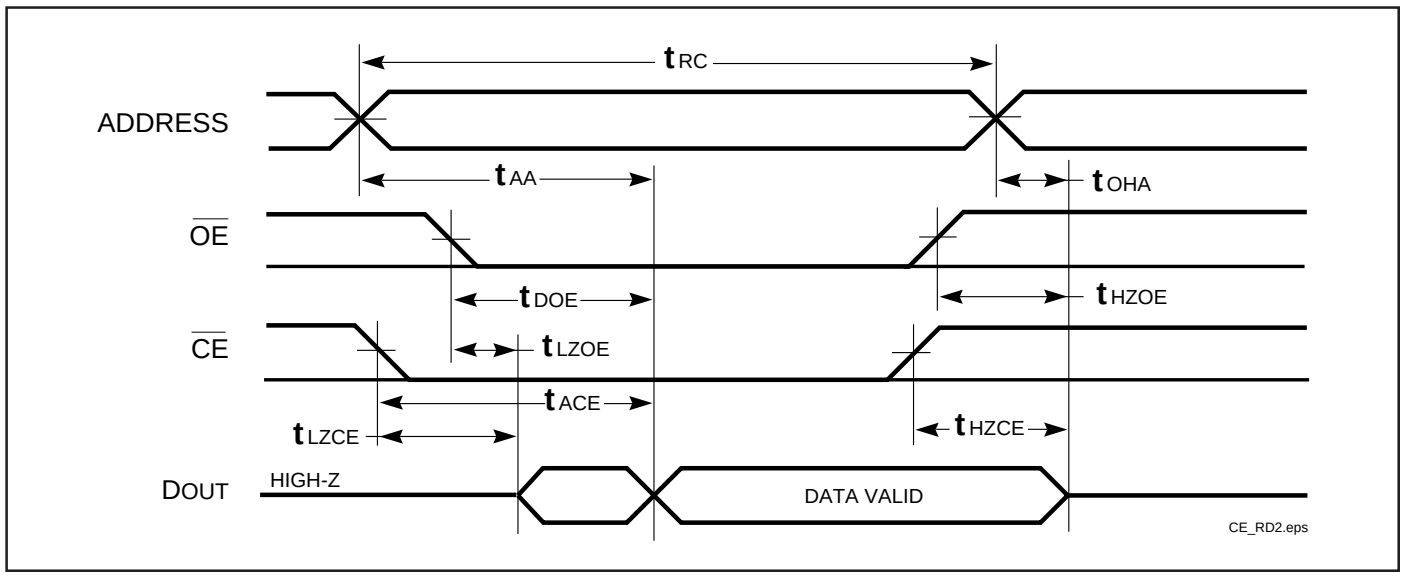
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

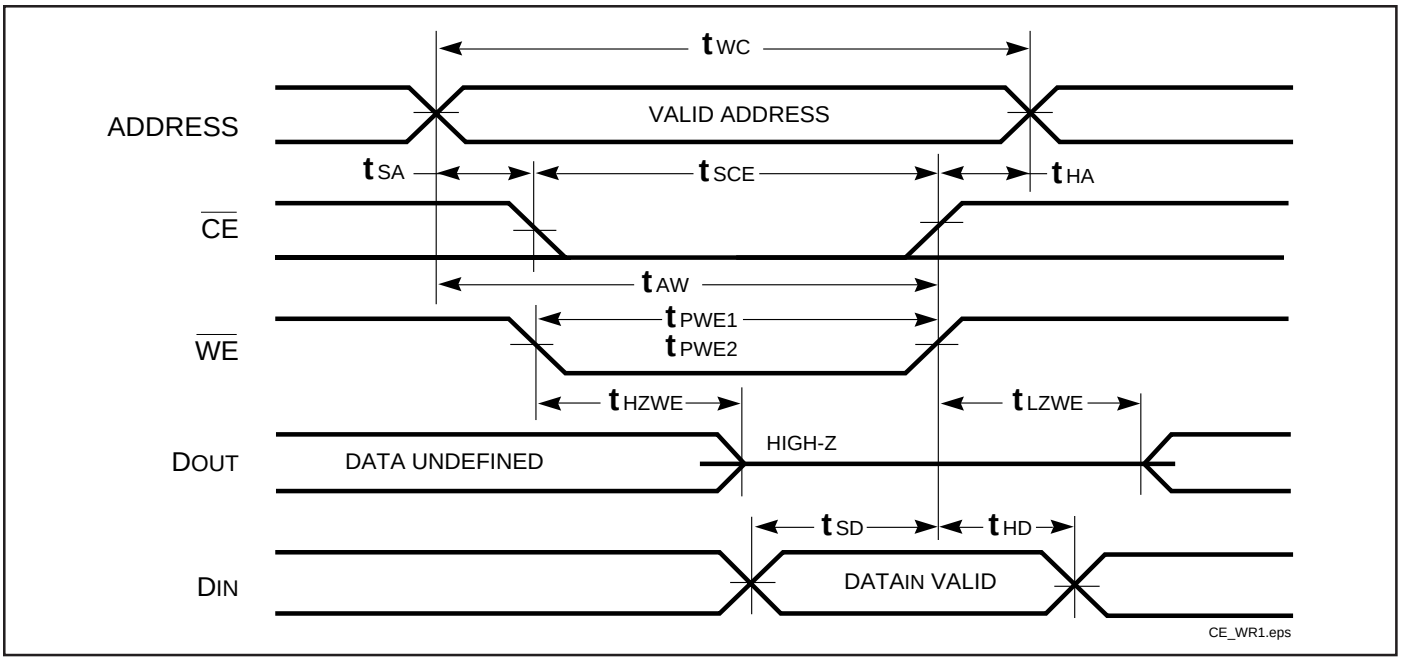
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

		-8 ns		-10 ns		-12 ns		-15 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	8	—	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	7	—	8	—	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	7	—	8	—	9	—	10	—	ns
t_{SD}	Data Setup to Write End	4.5	—	6	—	6	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	0	4	0	5	0	6	0	7	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

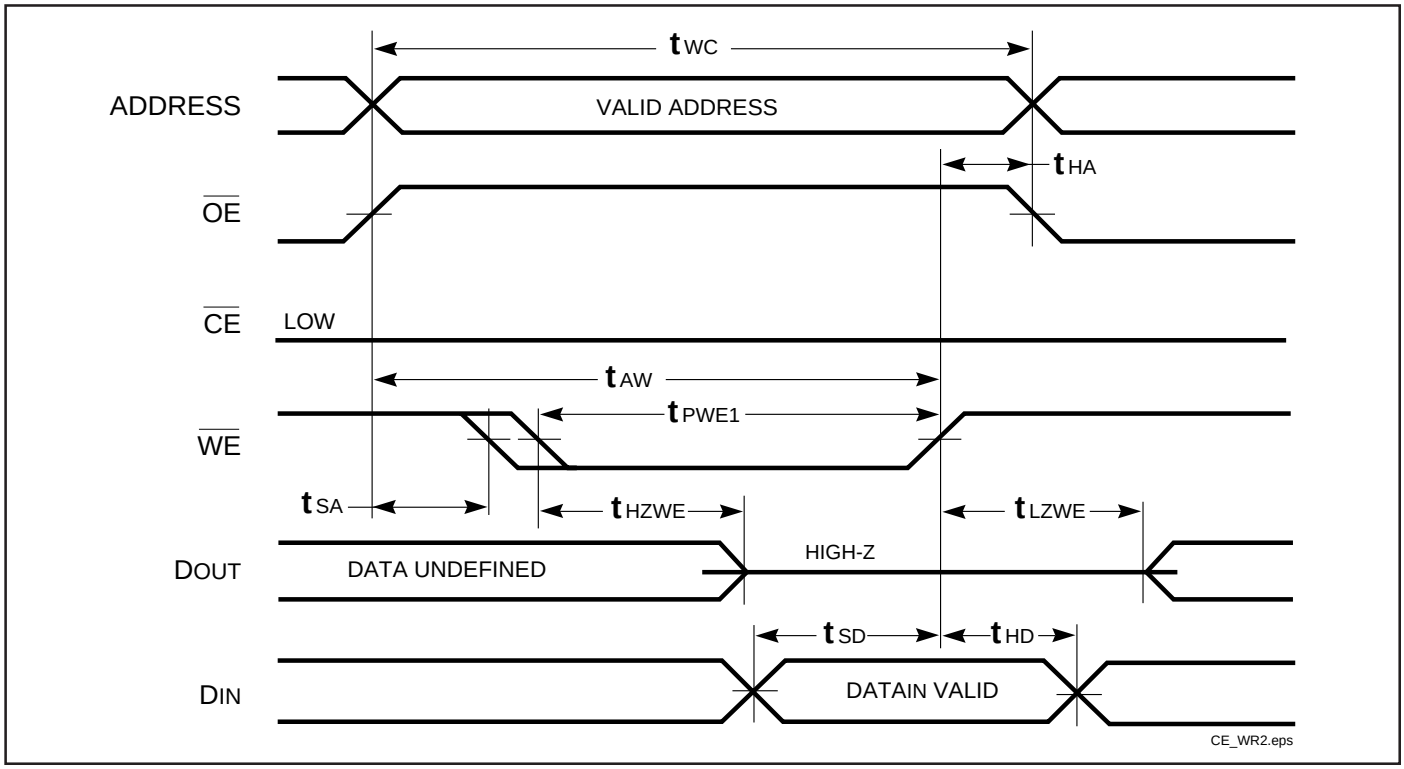
Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

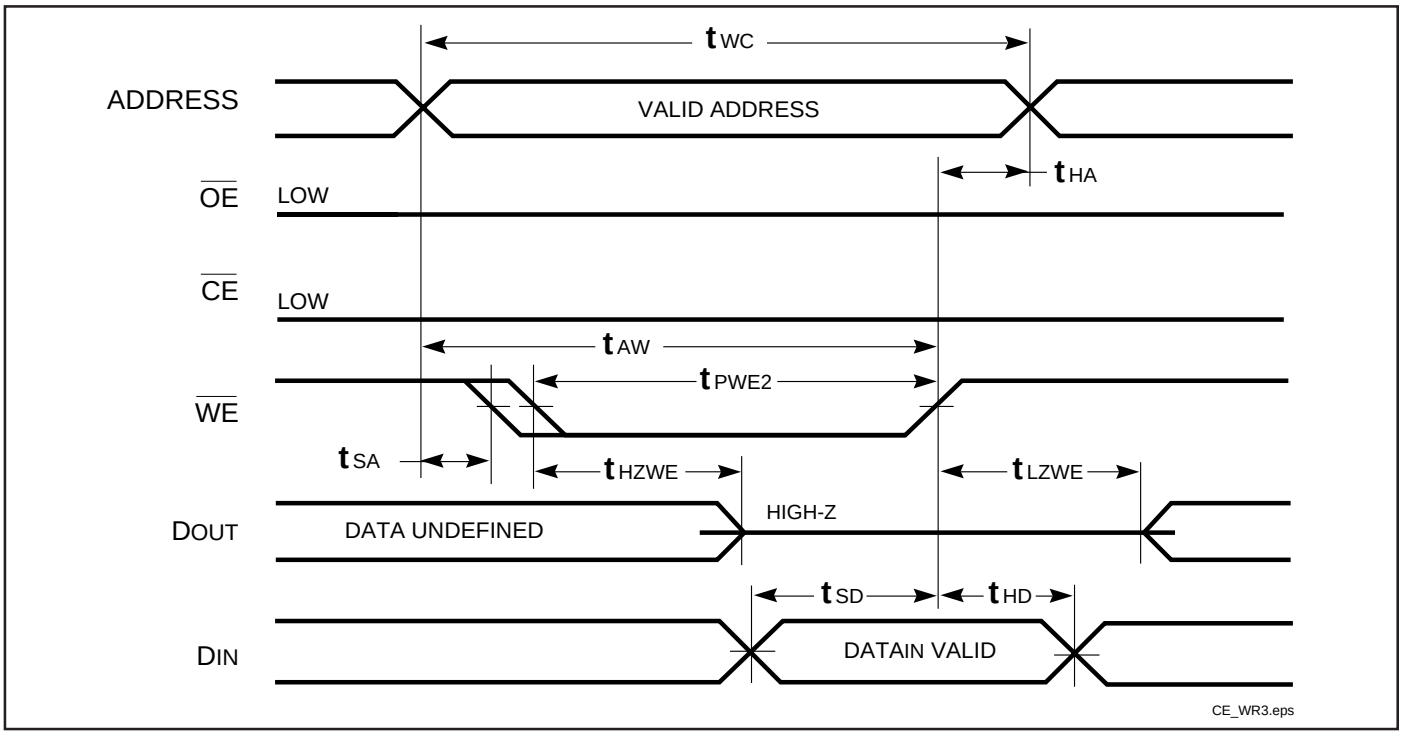
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed(ns)	Order Part No.	Package
8	IC63LV1024-8B	6*8mm TF-BGA
8	IC63LV1024-8H	8*13.4mm TSOP-1
8	IC63LV1024-8T	400mil T SOP-2
8	IC63LV1024-8J	300mil SOJ
8	IC63LV1024-8K	400mil SOJ
10	IC63LV1024-8B	6*8mm TF-BGA
10	IC63LV1024-8H	8*13.4mm TSOP-1
10	IC63LV1024-10T	400mil T SOP-2
10	IC63LV1024-10J	300mil SOJ
10	IC63LV1024-10K	400mil SOJ
12	IC63LV1024-8B	6*8mm TF-BGA
12	IC63LV1024-8H	8*13.4mm TSOP-1
12	IC63LV1024-12T	400mil T SOP-2
12	IC63LV1024-12J	300mil SOJ
12	IC63LV1024-12K	400mil SOJ
15	IC63LV1024-8B	6*8mm TF-BGA
15	IC63LV1024-8H	8*13.4mm TSOP-1
15	IC63LV1024-15T	400mil T SOP-2
15	IC63LV1024-15J	300mil SOJ
15	IC63LV1024-15K	400mil SOJ

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed(ns)	OrderPartNo.	Package
8	IC63LV1024-8BI	6*8mm TF-BGA
8	IC63LV1024-8HI	8*13.4mm TSOP-1
8	IC63LV1024-8TI	400mil T SOP-2
8	IC63LV1024-8JI	300mil SOJ
8	IC63LV1024-8KI	400mil SOJ
10	IC63LV1024-8BI	6*8mm TF-BGA
10	IC63LV1024-8HI	8*13.4mm TSOP-1
10	IC63LV1024-10TI	400mil T SOP-2
10	IC63LV1024-10JI	300mil SOJ
10	IC63LV1024-10KI	400mil SOJ
12	IC63LV1024-8BI	6*8mm TF-BGA
12	IC63LV1024-8HI	8*13.4mm TSOP-1
12	IC63LV1024-12TI	400mil T SOP-2
12	IC63LV1024-12JI	300mil SOJ
12	IC63LV1024-12KI	400mil SOJ
15	IC63LV1024-8BI	6*8mm TF-BGA
15	IC63LV1024-8HI	8*13.4mm TSOP-1
15	IC63LV1024-15TI	400mil T SOP-2
15	IC63LV1024-15JI	300mil SOJ
15	IC63LV1024-15KI	400mil SOJ

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